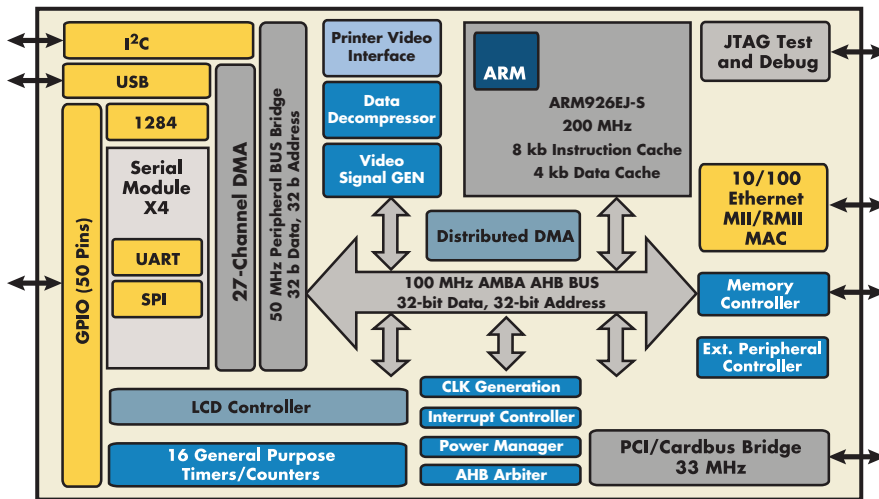


NS9775

352-Pin BGA; Lead-Free, RoHS Compliant



- 32-bit, 200 MHz, NET+ARM processor
- Video interface and JBIG for raster color printers
- Extensive on-chip peripherals
- Comprehensive networking software



Features/Benefits

High-performance 32-bit processor provides compute bandwidth for networked raster printer applications

- 200 MHz ARM9 core (ARM926EJ-S)
- Harvard architecture with 8 k/4 k instruction/ data cache
- DSP instruction set extensions
- Jazelle® Java byte-code accelerator

High level of peripheral integration provides glueless interfaces to a rich set of industry standard devices

- Full-duplex 10/100Base-T Ethernet MAC
- 100 MHz memory/peripheral controller
- PCI/Cardbus port
- High-resolution LCD controller
- USB 2.0 full-speed OHCI host or device
- Four multifunction serial ports: UART or SPI (master or slave)
- I²C port (master or slave)
- Programmable timers/counters available on I/O
- Fifty General-Purpose I/O (GPIO) pins
- Highly configurable power management

Application specific hardware for tandem or multipass laser engines

- 4 parallel video raster channels, each includes a hardware JBIG decoder
- 4-channel glueless video interface

Supported by the comprehensive and integrated NET+Works® development suite

Overview

The NS9775 is a high-performance, one-chip controller designed for color laser printers and segment 1 and 2 multifunction devices. The device integrates an ARM926EJ-S processor core, memory and I/O support with four independent video channels, each incorporating hardware JBIG decompression. I/O support includes 10/100Base-T Ethernet, USB, IEEE 1284 and serial ports. With an internal LCD controller and PCI/CardBus interface, the NS9775 contains most of the major functional components for color printer or MFP controllers accepting a compressed-raster data format.

Its four video channel capability is a unique feature that provides direct drive for tandem (one pass) marking engines. The NS9775 also allows for multi-bits per pixel support of multi-pass marking engines and for simplified drive of the next generation of dual beam marking engines.

Printer and MFP controllers must move large amounts of data in real time between the external I/O ports and the marking or scanning engines. The NS9775 architecture provides multiple bus masters/distributed DMA which, along with programmable bus management, allows it to set up multiple paths to simultaneously move print or scan information with minimal CPU intervention.

Controllers based on the NS9775, with suitable host drivers, can drive color printers as fast as 90 pages per minute (A4/letter size, 600x600 dpi), while costing significantly less than traditional printer controllers.

Please contact us at 1-877-OEM-DIGI or 952-912-3444 for additional information or to discuss your specific application requirements.

Hardware Specifications

32-BIT ARM926EJ-S RISC PROCESSOR

- 200 MHz
- 5-stage pipeline
- Harvard architecture
- 8 kB I-Cache and 4 kB D-Cache
- 32-bit ARM and 16-bit Thumb instruction sets, can be mixed for performance/code density tradeoffs
- MMU to support virtual memory based OS's such as Linux, WinCE/Pocket PC, VxWorks, others
- DSP instruction extensions, improved divide, single cycle MAC
- ARM Jazelle, 1200 CM (Coffee Marks) Java Accelerator
- Embedded ICE-RT debug unit
- JTAG boundary scan, BSDL support

PRINT ENGINE CONTROLLER

- 4 parallel JBIG decoders
 - Internal bypass for uncompressed data
 - Automatic and manual header processing modes
- Glueless interface to most print engines
 - 4 data ports for color tandem printers
 - Single port for 4-pass color printers
 - Single port for monochrome printers
- Up to 13" lines at 2400 dpi
- High print speed:
 - Tandem: 90 ppm
 - 4-pass color: 22 ppm
 - Monochrome: 90 ppm
- At these conditions below:
 - Page size: 8.5" x 11"
 - Resolution: 600 x 600 dpi
 - Video clock: 100 MHz
 - Horizontal correction factor: 0.7
 - Vertical correction factor: 0.7
- Asynchronous print mode with internal PLL
 - Clock rates up to 100 MHz
- Synchronous print mode with 1 or 4 external clocks
 - Clock rates up to 200 MHz
- Bus Master on the system bus and a dedicated 4-channel DMA engine, one per color plane
- On-chip input and output FIFOs, one pair per color plane
- General communication through serial and GPIO ports

EXTERNAL BUS SYSTEM INTERFACE

- 32-bit data bus, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- Up to 256 MB SDRAM, up to 2 GB DIMM
- 4 static and 4 dynamic memory chip selects
- 0-63 wait states per chip select
- Self-refresh during system sleep mode
- Automatic dynamic bus sizing to 8-bits, 16-bits, 32-bits
- Burst-mode support with automatic data width adjustment

SYSTEM BOOT

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

OPTIMIZED 10/100 ETHERNET MAC

- 10/100 Mbps MII/RMII PHY interfaces
- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kb RX FIFO
- 256 byte Tx FIFO with on-chip buffer descriptor ring
 - Eliminates underruns and decreases bus traffic
- Separate Tx and Rx DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering
- External CAM filtering

PCI/CARDBUS SUPPORT

- PCI v.2.2, 32-bit bus, up to 33 MHz bus speed
- Programmable to:
 - PCI device mode
 - PCI host mode: supports up to 3 external PCI devices
 - CardBus host mode

FLEXIBLE LCD CONTROLLER

- Supports most commercially available displays
 - Active Matrix color TFT displays: up to 24 bpp direct 8:8:8 RGB; 16 M colors
 - Single- and dual-panel color STN displays: up to 16 bpp 4:4:4 RGB; 3375 colors
 - Single- and dual-panel monochrome STN displays: 1, 2, 4 bpp palettized gray scale
- Formats image data and generates timing control signals
- Internal programmable palette-LUT and grayscale support different color techniques
- Programmable panel-clock frequency

USB PORTS

- USB v.2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps)
- Configurable to device or OHCI host
 - USB host is a bus master
 - USB device supports one bi-directional control endpoint and 11 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel; 13 total
- 20 B Rx FIFO and 20 B Tx FIFO

Hardware Specifications

SERIAL PORTS

- 4 serial modules, each independent configurable to UART mode, SPI Master mode, or SPI Slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 6.25 Mbps: synchronous mode
- UART provides
 - High-performance hardware and software flow control
 - Odd, even, or no parity
 - 5, 6, 7 or 8 bits
 - 1 or 2 stop bits
 - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for Rx clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte Tx FIFO and 32 byte Rx FIFO per module

I²C PORT

- I²C v.1.0, configurable to Master or Slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I²C bus arbitration

SYSTEM BUS

- Power save during normal operation
 - Disables unused modules
- Power save during sleep mode
 - Sets SDRAM to self-refresh mode
 - Disables all modules except selected wakeup modules
 - Wakeup on valid packets or characters
- Patent pending technology

1284 PARALLEL PERIPHERAL PORT

- All standard modes:
 - ECP, Byte, Nibble, Compatibility
- RLE (Run Length Encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

SYSTEM BUS

- Every system bus peripheral is a bus master with dedicated DMA engine
- Deterministic bus bandwidth allocation (patent pending)

PERIPHERAL BUS DMA

- One 13-channel engine supports USB device
 - 2 DMA channels support control endpoint
 - 11 DMA channels support 11 endpoints
- One 12-channel engine supports
 - 4 serial modules (8 DMA channels)
 - 1284 parallel ports (4 DMA channels)
- All DMA channels support fly-by mode

EXTERNAL PERIPHERAL DMA

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

POWER MANAGEMENT

- Power save during normal operation
 - Disables unused modules
- Power save during sleep mode
 - Sets memory controller to refresh
 - Disables all modules except selected wakeup modules
 - Wakeup on valid packets or characters
- Patent pending

VECTOR INTERRUPT CONTROLLER

- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

GENERAL PURPOSE TIMERS/COUNTERS

- 16 independent 16-bit or 32-bit programmable timers or counters
 - Each has an I/O pin
- Mode selectable into:
 - Internal timer mode
 - External gated timer mode
 - External event counter
- Timers/counters can be concatenated
- Resolution to measure minute-range events
- Source clock selectable
 - Internal clock or external pulse event
- Individually enabled/disabled

SYSTEM TIMERS

- Watchdog timer
- System bus monitor timer
- System bus arbiter timer

GENERAL PURPOSE I/O

- 50 programmable GPIO pins (muxed with other functions)
- Software-readable power-up status registers for every pin for customer-defined bootstrapping

EXTERNAL INTERRUPTS

- 4 external programmable interrupts
 - Rising- or falling-edge sensitive
 - Low- or high-level sensitive

CLOCK GENERATOR

- Low-cost external crystal
- On-chip phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate oscillator for USB

OPERATING FREQUENCY

- 133 MHz, 0° C to 70° C
- 162 MHz, 0° C to 70° C
- 200 MHz, 0° C to 70° C

OPERATING VOLTAGE

- Core: 1.5V ± 0.1V
- I/O ring: 3.3V ± 10%

POWER CONSUMPTION

- 200 MHz:
 - Max: 1.7 W (estimated)
 - Typical: 950 mW (measured)

PACKAGE

- 352-pin BGA
- 1.27 mm ball pitch
- 35.0 mm x 35.0 mm
- Lead-free; RoHS compliant

NET+Works Integrated Software

NET+ARM network attached processors are the core of the NET+Works family of solutions that add intelligence and connectivity to electronic devices. We offer extensive networking software to support industrial automation, building automation, point-of-sale, office automation and other enterprise applications.

DEVELOPMENT TOOLS

- ThreadX® picokernel RTOS
- Green Hills® MULTI® IDE or Microcross GNU X-Tools™
- Drivers (10/100Base-T Ethernet, UART, SPI, I²C, DMA, flash, USB host & device, LCD, PCI)

NETWORKING PROTOCOLS

- TCP/IP stack
- TCP and UDP Sockets API
- ICMP
- IGMP
- PPP for serial communications
- RARP
- ARP Ping
- Link-Local addressing AutoIP
- DHCP client
- BootP
- Fast IP
- Fast sockets
- SSL, TLS

NETWORKING SERVICES

- FTP server
- FTP client
- LDAP agent, for access to network information services
- HTTP APIs for serving basic advanced web pages, HTTPS for security
- Email (POP and SMTP)
- SNMP v1/MIBII for remote management
- SNTp
- DNS
- Telnet
- Multi-homing

UTILITIES

- HTML compilation
- MIB compilation
- Download of Flash images
- Code builds
- Integrated Flash file system
- Code profiler
- Boundary Scan Description Language (BSDL)
- Network printer discovery application services

OPTIONAL PRINT SERVICES

- DPO/ES print server interface
- Compatible print servers
 - LPD
 - LPP
 - Raw sockets
 - USB
 - IEEE 1284
 - FTP
 - POP3
- IPX/SPX protocol and Novell Pserver
- Apple EtherTalk and support protocols including PAP
- SLP with printer template
- Digi print server MIB
- Video-channel pipelining module

TECHNICAL SUPPORT

- One year of software maintenance and technical support

DEVELOPMENT BOARD

- NS9775 development board and JTAG Probe

MODEL.....PART NUMBERS

Model
200 MHz, 0° C to 70° C

Worldwide
NS9775B-0-C20

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Digi International, the leader in device networking for business, develops reliable products and technologies to connect and securely manage local or remote electronic devices over the network or via the web. With over 20 million ports shipped worldwide since 1985, Digi offers the highest levels of performance, flexibility and quality.

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