ConnectCore 6UL

Hardware Design Guidelines and Checklist

Revision history—90002341

Revision	Date	Description
A	June 2019	Initial release
B	April 2020	Corrected minor power rail name errors and typos

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- Firmware version
- Operating system/browser (if applicable)
- Logs (from time of reported issue)
- Trace (if possible)
- Description of issue
- Steps to reproduce

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Contents

About this document

Overview

The purpose of this document is to ease and drive the hardware design process of ConnectCore 6UL SOM-based products. Schematics milestones keep bring-up of your designs on track for success, and layout recommendations help achieve optimal electrical behavior.

This document, together with the ConnectCore 6UL System-on-Module Hardware Reference Manual, provide information key to ensuring a functional, quality design featuring the ConnectCore 6UL module.

Naming and signal conventions

This document is written assuming the reader has a good working knowledge of common electronics terminology. You may also encounter the following specific conventions:

Convention	Definition
signal_name#	A hash sign at the end of a signal name denotes that it is an active low signal.
_B	An alternate way to indicate a signal is active low.
x	Indicates an alphanumeric value.
Register/signal [a:b]	Brackets after a name refer to the bits or signals contained in a register, or in a set of related signals.

Schematics design checklist

The microprocessor used on this module, like all CMOS devices, can be driven into a latch-up condition if any I/O pin is driven outside of its associated power rail. Care must be taken to:

- Never drive an I/O pin beyond its positive rail or below ground.
- Never drive an I/O pin from an external power source during the power-on or reset sequences.
- Never hot-swap the module or interrupt its ground connection to external circuitry.

Latch-up is a condition that can cause excessive current draw and result in excessive heating of the microprocessor or its power supplies. This excessive heating can permanently damage the microprocessor and/or its supporting components.

<table>
<tr><th>☑</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">Power supply</td></tr>
<tr><td></td><td>1. Input power of the SOM</td><td>Make sure the input power supply of the module follows one of the two available configurations:

<table>
<tr><th></th><th>VSYS</th><th>LDOG</th><th>VPWR</th></tr>
<tr><td>With front-end LDO</td><td>Connected to Mosfet drain</td><td>Connected to Mosfet gate</td><td>Input power line: 4.6V - 5.5V</td></tr>
<tr><td>Without front-end LDO</td><td>Input power line: 3.7V - 4.5V</td><td>Floating</td><td>Grounded</td></tr>
</table>

Note For detailed information about the input power circuitry, see the ConnectCore 6UL System-on-Module Hardware Reference Manual.</td></tr>
</table>

☑	Item	Description
	2. Minimum decoupling capacitors on VSYS/VSYS2	2 x 47uF + 1 x 4.7uF + 1 x 100nF
	3. VCC_MCA power line	This power line is the input power supply of the on-module MCA. It must be powered from a dedicated 3.3V regulator connected to the main input power supply of the board, since it is an always-on power supply. Connect a Schottky diode (low forward voltage drop) between the output of the regulator and the VCC_MCA pin. VIN_PRESENT must be tied to the output of this 3.3V regulator. To allow coin-cell (low-power mode) applications, the coin-cell/supercap must be connected to VCC_MCA again through a Schottky diode. See Schematic: coin-cell/supercap connected to VCC_MCA through Schottky diode. **Note** In the ConnectCore 6UL reference designs (SBC PRO and SBC Express) there's a 100 Ω series resistor between the coin-cell/supercap and VCC_LICELL signal in the circuit above. Please remove this resistor. It introduces a voltage drop in the transitory from normal operation to RTC mode operation which could cause undesirable RTC behavior.
	4. 3V3_EXT power rail	3V3_EXT is a dedicated 3.3V output power rail for powering external circuitry of the carrier board. Do not connect any external power supply to this line.
	5. VCC_ENET power rail	VCC_ENET is a 3.3V input power rail for supplying the ENET module of the CPU. Digi recommends you feed this power domain directly from the 3V3_EXT power rail.
	6. Unconnected power rails	By default, leave the following power rails unconnected: • VCC_NAND (pad C12) • VDDA_ADC_3P3 (pad L3) • VDD_SNVS_3V3 (pad D12) • VCC_LICELL (pad B1) • 3V3_INT (pad E3) Although these signals are not used externally, it may be helpful to leave them accessible for debugging (test points).

<table>
<tr><th>☑</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">BOOT</td></tr>
<tr><td></td><td>1. BOOT_MODE [1:0]</td><td>These lines select the boot mode of the SOM:

<table><tr><th>BOOT_MODE1</th><th>BOOT_MODE0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Boot from fuses</td></tr><tr><td>0</td><td>1</td><td>Serial downloader</td></tr><tr><td>1</td><td>0</td><td>Boot from board settings</td></tr><tr><td>1</td><td>1</td><td>Reserved</td></tr></table>
By default, select the Boot from board settings option to boot from the internal NAND memory. Use 10K resistors for pulling these line up or down. When pulled-high, refer these lines to VDD_SNVS_IN. When this is not possible (castellated pad configuration), use the 3V3_EXT power line.

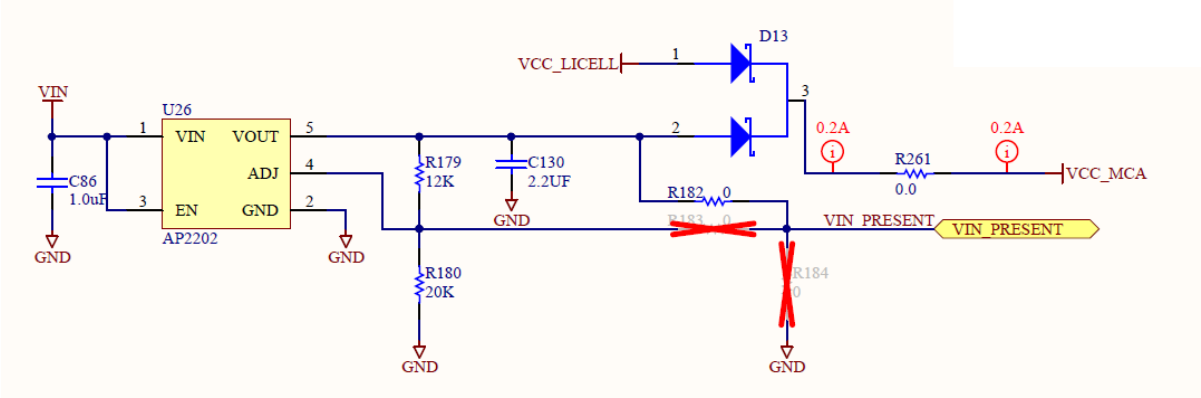
Note BOOT_MODE0 is internally pulled-low. In the castellated version, only BOOT_MODE1 is available externally.</td></tr>
<tr><td></td><td>2. Recover/Debug mode (USB)</td><td>To allow the system to boot from USB as a recovery/debug method, add a jumper for shorting BOOT_MODE1 line to GND. This will force the system to boot from fuses, and as long as they are not burned, the system will fall into serial mode and boot from USB. This method is faster than changing both BOOT_MODE[1:0] lines resistors to set up the Serial Downloader, and can be helpful during the development phase when you do not want to burn fuses.
The CPU can only boot from the USB_OTG1 bus. (USB_OTG2 is not bootable.)</td></tr>
<tr><td></td><td>3. Boot configuration lines</td><td>Make sure the BOOT_CFG1[7:0] lines are properly setup for booting from the on-module NAND memory:
LCD_DATA0 (BOOT_CFG1[0]): pull-down
LCD_DATA1 (BOOT_CFG1[1]): pull-down
LCD_DATA2 (BOOT_CFG1[2]): pull-down
LCD_DATA3 (BOOT_CFG1[3]): pull-down
LCD_DATA4 (BOOT_CFG1[4]): pull-up
LCD_DATA5 (BOOT_CFG1[5]): pull-down
LCD_DATA6 (BOOT_CFG1[6]): pull-down
LCD_DATA7 (BOOT_CFG1[7]): pull-up
Use 10K resistors to pull these line up or down. When pulled-high, refer these lines to 3V3_EXT.</td></tr>
</table>

☑	Item	Description
	4. Boot configuration lines buffer	Boot configuration lines are latched during booting for configuring the boot process of the SOM. Digi recommends you add a buffer to protect these lines during booting. External circuitry and peripherals connected to these lines can modify the expected value when system is booting, so that the process can fail. See the Schematic: boot configuration lines used on the ConnectCore 6UL SBC PRO reference design. Eight additional BOOT_CFG lines are configured inside the module. These lines are LCD_DATA[9:15]. Place another buffer for these lines if you expect to have external circuitry/peripherals modifying their values.
	5. LCD_DATA23 line configuration	This line is one of the GPIOs latched during booting and is used to configure one of the Boot Configuration bits (BOOT_CFG4[7]). It enables an infinite loop debug mode. For proper operation, make sure this line is not pulled-high during booting.
MCA		
	1. MCA_RESET	Input reset line of the system. Connect a 100K pull-up to VCC_MCA.
	2. SWD_ CLK/PWR_IO	Input power on/off - suspend line of the system. Connect a 100K pull-up to VCC_MCA.
	3. Isolate VCC_ MCA power domains	As much as possible, try not to mix the VCC_MCA power domain with the rest of the power domains of the system. The ConnectCore 6UL SBC Express/PRO designs use an MCA GPIO to manage the reset line of the LAN8720Ai PHY (powered from 3V3_EXT). This configuration resulted in some unexpected backdrive currents.
Console debug port		
	1. UART5	The default U-Boot loaded in the modules from manufacturing configures the UART5 as the console debug port. This console port can be changed to any other UART in the system, but Digi recommends you use this UART5 as the console port so no additional effort (such as compiling a new U-Boot, loading it through USB, etc.) are required.
I2C		
	1. I2C1 bus	Do not use the I2C1 bus to communicate with external peripherals. This bus is used internally in the module for interconnecting critical devices (CPU, MCA, PMIC).
	2. I2C pull-ups	Add external pull-ups to the clock and data lines of the I2C buses. You will typically use 4.7K resistors.
GPIOs		
	1. GPIO5 port	GPIO5_x I/Os are supplied from VDD_SNVS_IN (3.0V). Do not overdrive them with 3.3V.

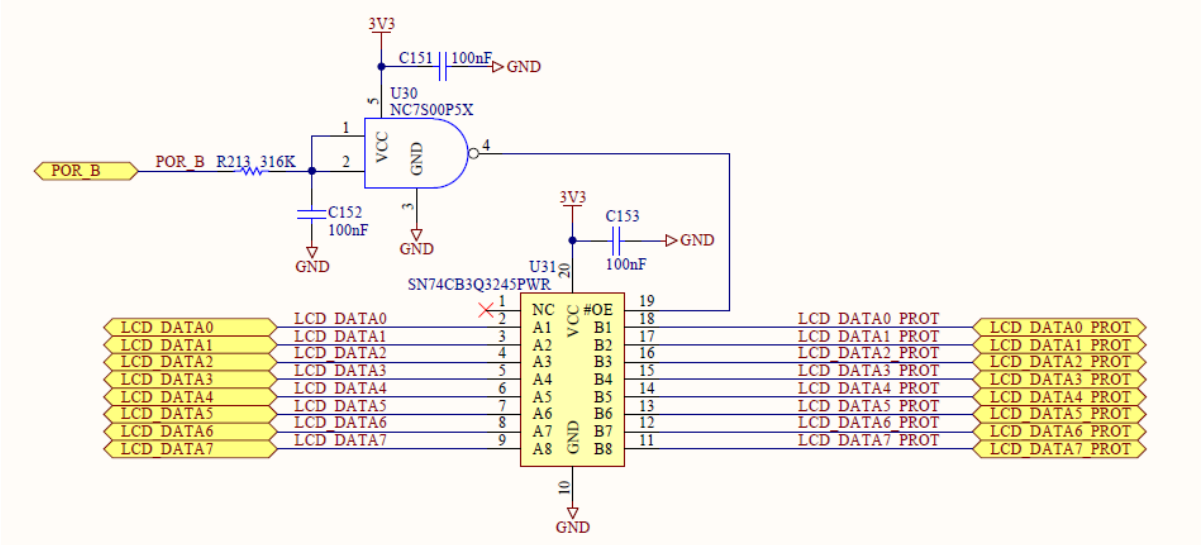
☑	Item	Description
	2. GPIO5_03	GPIO5_03 (pad V15) is not supported.
NAND		
	1. NAND signals	The following pads, which are used internally, must be left unconnected if you want to use the on-module NAND flash memory: • B10 (NAND_CE#) • B8 (NAND_CLE) • B9 (NAND_ALE) • B11 (NAND_WE#) • C9 (NAND_RE#) • C10 (NAND_WP#) • D11 (NAND_READY#) • C6 (NAND_DATA0) • C7 (NAND_DATA1) • C8 (NAND_DATA2) • M3 (NAND_DATA3) • D6 (NAND_DATA4) • N2 (NAND_DATA5) • R2 (NAND_DATA6) • C15 (NAND_DATA7)
Wireless and Bluetooth		
	1. Wireless SDIO	The SDIO1 interface of the CPU is used internally in the SOM for the wireless connectivity. The following pads must be left unconnected to preserve this wireless functionality: • K19 (WLAN_SD1_CLK) • L19 (WLAN_SD1_CMD) • M19 (WLAN_SD1_DATA0) • L20 (WLAN_SD1_DATA1) • K20 (WLAN_SD1_DATA2) • M20 (WLAN_SD1_DATA3) This applies only to Wireless variants of the SOM. In non-wireless variants, the SDIO1 bus is available.

☑	Item	Description
	2. Bluetooth UART	The UART1 port of the CPU is used internally in the SOM for Bluetooth connectivity. The following pads must be left unconnected to preserve this Bluetooth functionality: • D17 (BT_UART1_TX) • D16 (BT_UART1_CTS#) • D18 (VT_UART1_RX) • D19 (BT_UART1_RTS#) This applies only to Wireless variants of the SOM. In non-wireless variants, the UART1 bus is available.
	3. Not supported functionality	Functionality associated with the following pads is not currently supported: • B17: WLAN_RF_KILL# • B18: BT_RF_KILL# • B19: WLAN_LED • B20: BT_LED
	4. External antenna	See RF guidelines.
CPU control lines		
	1. POR_B	POR_B is the reset line of the CPU. It is managed internally. It can be used as an output for managing (resetting) external circuitry of the carrier board, but it must never be driven as an input. Even though this signal is not used externally, it may be useful to have it accessible for debugging (test point).
	2. ONOFF	By default, let this pad unconnected.
	3. PWR_ON	Similar as the POR_B signal, this line is driven internally in the SOM. It is the PMIC ON/OFF signal. It can be used externally for managing external circuitry but must never be driven as an input. Although this signal is not used externally, it may be helpful to leave it accessible for debugging (test points).

Schematic: coin-cell/supercap connected to VCC_MCA through Schottky diode



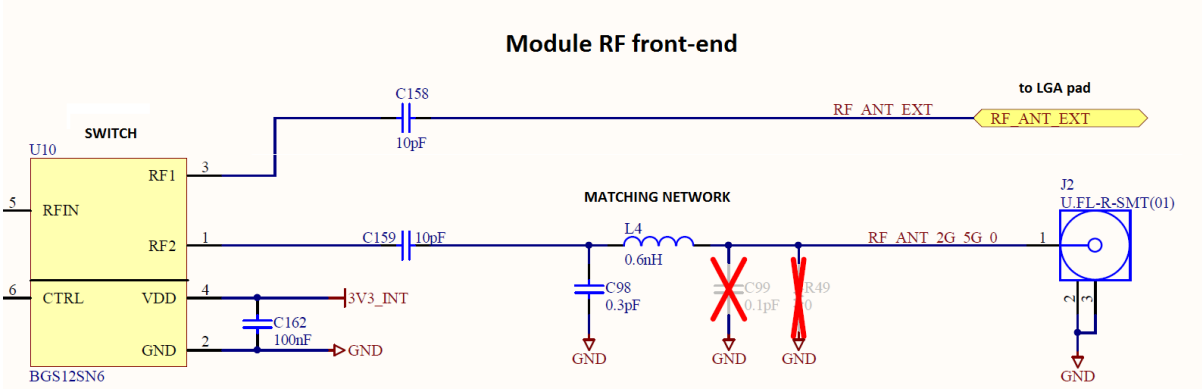
Schematic: boot configuration lines used on the ConnectCore 6UL SBC PRO reference design



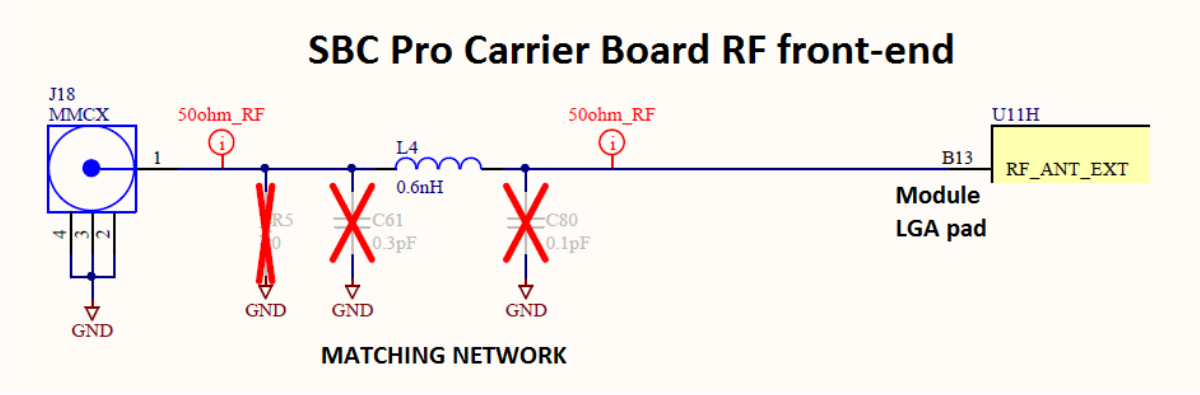
RF guidelines

RF matching network for the external antenna

On the bottom side of the module, there is an LGA pad that can be used to route the RF path from the QCA6564A wireless chip, out the top of the customer carrier board. A digital switch selects between routing the RF path either to the U.FL connector or to this LGA pad, named RF_ANT_EXT.



The RF_ANT_EXT comes directly (AC coupled by a cap) from the digital switch because the matching network implemented at the RF path for the U.FL connector is not present. Instead, it is assumed that this matching network will be located on the carrier board to compensate for the mismatching introduced when routing from the LGA pad to the carrier board.



The RF output power at the U.FL connector has been calibrated based on its current matching network. Via stored tables on the firmware, a flat RF output power over frequency is provided at the U.FL connector. (That is, the same amount of power is delivered at each frequency over the band.)

Since the matching is different for the external antenna at the LGA pad, this RF output power calibration in the firmware is not valid and a new calibration data should be generated based on matching from the LGA pad to an external antenna. When the current calibration data based on the U.FL connector is applied to the external antenna as routed on the SBC Pro carrier board from Digi, the RF power levels are slightly lower, and also waved along frequency. If applied on another external antenna on another carrier board design, the resulting RF power levels will depend directly on the implemented matching network.

Regulations

Both antennas have been certified compliant, assuming the external is connected as in the SBC Pro carrier board from Digi. For an external antenna on another carrier board design to remain compliant, the same design approach must be followed to reduce conformance testing to a spot-check. Certification testing can also be reduced by using already-approved antennas by Digi. You can also use antennas of the same kind with equal or less gain to reduce testing.

Bring-up guidelines

This section offers guidelines for performing bring-up of a ConnectCore 6UL-based product.

Power-up

The very first power-up of a product is one of the most critical step of the bring-up. Use a power supply with current limiter so the system is protected in case an unexpected short (or any other high-current incident) occurs. The ConnectCore 6UL SOM will not have a static power consumption higher than 120-130 mA from factory mode (except booting peaks). So, together with the expected power consumption of the carrier board, you can estimate an upper limit for the current consumption in the bring-up.

Power rails

Once you have verified that the power consumption of the system is acceptable and no shorts are present, the next step is to verify that all power rails also have their expected voltage value. The following table tracks the voltage expected in the main power domains of the system:

Power rail	Expected voltage
VSYS/VSYS2	Depending on the power supply strategy used. See point 1 of the Power supply section under the Design Checklist chapter.
VCC_MCA	3V - 3.3V (Output of the 3.3V dedicated regulator minus Schottky diode forward voltage).
3V3_EXT	3.3V
3V3_INT	3.3V
VCC_NAND	3.3V
VDD_SNVS_IN	3.0V

If all these power rails are in compliance with their expected voltage value, it means that the system is completely powered. The PMIC has already initialized and the SOM should boot.

Verify system boot

If everything has gone right and the system has booted, you should be able to communicate with the SOM through the console port of the system. If this is not the case, check the following:

- Make sure the UART debug port lines are not crossed. Crossing the TX and RX lines of the console UART is a very common mistake.
- Verify the value of the BOOT_MODE lines.
- Verify the value of the BOOT_CONFIGURATION lines.
- Make sure LCD_DATA23 (BOOT_CFG4[7]) is not pulled-high.
- Verify that VIN_PRESENT is at high level (3.3V).
- Verify that POR_B signal is at high level.

Note For more information, see the ConnectCore 6UL System-on-Module Hardware Reference Manual.