ConnectCore 8X

Hardware Design Guidelines and Checklist

Revision history—90002394

Revision	Date	Description
A	April 2020	Initial release
B	May 2021	Updated POR_B description
C	March 2023	Updated schematic diagram

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- Firmware version
- Operating system/browser (if applicable)
- Logs (from time of reported issue)
- Trace (if possible)
- Description of issue
- Steps to reproduce

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About this document

Overview

The purpose of this document is to ease and drive the hardware design process of ConnectCore 8X SOM-based products. Schematics milestones keep bring-up of your designs on track for success, and layout recommendations help achieve optimal electrical behavior.

This document, together with the ConnectCore 8X System-on-Module Hardware Reference Manual, provide information key to ensuring a functional, quality design featuring the ConnectCore 8X module.

Naming and signal conventions

This document is written assuming the reader has a good working knowledge of common electronics terminology. You may also encounter the following specific conventions:

Convention	Definition
signal_name#	A hash sign at the end of a signal name denotes that it is an active low signal.
_B	An alternate way to indicate a signal is active low.
x	Indicates an alphanumeric value.
Register/signal [a:b]	Brackets after a name refer to the bits or signals contained in a register, or in a set of related signals.

Design checklist

The microprocessor used on this module, like all CMOS devices, can be driven into a latch-up condition if any I/O pin is driven outside of its associated power rail. Care must be taken to:

- Never drive an I/O pin beyond its positive rail or below ground.
- Never drive an I/O pin from an external power source during the power-on or reset sequences.
- Never hot-swap the module or interrupt its ground connection to external circuitry.

Latch-up is a condition that can cause excessive current draw and result in excessive heating of the microprocessor or its power supplies. This excessive heating can permanently damage the microprocessor and/or its supporting components.

Power supply

☑	Item	Description
	1. Minimum decoupling capacitors on VSYS/VSYS2	1 x 100 uF + 1 x 10 uF + 1 x 1 uF

☑	Item	Description
	2. Powering the MCA	This power line is the input power supply of the on-module MCA. It must be powered from a dedicated 3.3 V regulator connected to the main input power supply of the board, since it is an always-on power supply. Connect a Schottky diode (low forward voltage drop) between the output of the regulator and the VCC_MCA pin. MCA_VIN_DET must be tied to the output of this 3.3 V regulator[1]. To allow coin-cell (low-power mode) applications, the coin-cell/supercap must be connected to VCC_MCA again through a Schottky diode. See Coin-cell/supercap connected to VCC_MCA through Schottky diode. Ensure there is no series resistance between the coin-cell/supercap and the VCC_LICELL net in the circuit linked above. It introduces a voltage drop in the transitory from normal operation to RTC mode operation which could cause undesirable RTC behavior. [1]*Digi has validated that using a comparator instead of a direct connection drastically improves the transitory time that the system takes to go from normal operation to RTC mode. See Comparator used for connecting MCA_VIN_DET line used on the ConnectCore 8M Nano DVK.*
	3. Output power rails	The following power rails are outputs from the ConnectCore 8X SOM: ■ 3V3 ■ 1V8 ■ LDO3 ■ LDO4 ■ VCC_SCU_1V8 These power rails (except VCC_SCU_1V8, which must only power the boot mode and JTAG circuitry) are intended to power external circuitry on the carrier board. Do not connect any external power supply to these lines.
	4. Input power rails	The following power rails are inputs to the ConnectCore 8X SOM: ■ LDO3IN ■ LDO4IN ■ VDD_USDHC1 ■ VDD_MIPI_DSI_DIG ■ VDD_ENET0 ■ VDD_ESAI_SPDIF ■ VDD_SPI_SAI ■ VDD_QSPI0B ■ VDD_CSI Digi recommends using the module output power rails to power these power domains of the SOM.

☑	Item	Description
	5. Unconnected power rails	By default, leave the following power rails unconnected: ■ VCC_SNVS_LDO_1V8 ■ VDD_PCIE_DIG ■ VDD_EMMC0 ■ NVCC_MIPI_CSI_DSI Although these signals are not used externally, it may be helpful to leave them accessible for debugging (test points).

Boot

☑	Item	Description
	1. BOOT_MODE [1:0]	These lines select the boot mode of the SOM: <table><tr><th>BOOT_MODE1</th><th>BOOT_MODE0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Boot from fuses</td></tr><tr><td>0</td><td>1</td><td>Serial downloader</td></tr><tr><td>1</td><td>0</td><td>Boot from board settings</td></tr><tr><td>1</td><td>1</td><td>Reserved</td></tr></table> Digi recommends you configure the boot mode lines to boot by default from the internal eMMC of the module. This means: ■ BOOT_MODE0 pulled-down through 100 K resistor ■ BOOT_MODE1 pulled-high through 4.7 K resistor See the ConnectCore 8X System-on-Module Hardware Reference Manual for detailed information about the boot modes available on the SOM. **Note** BOOT_MODE0 is internally pulled-low. In the castellated version, only BOOT_MODE1 is available externally.
	2. Recover/Debug mode (USB)	To allow the system to boot from USB as a recovery/debug method, Digi recommends you add switches to quickly switch between the different boot modes. See Boot mode switches for selecting the boot source of the module.

MCA

☑	Item	Description
	1. MCA_ RESET	Input reset line of the system. Connect a 100 K pull-up to VCC_MCA.
	2. SWD_ CLK/PWR_IO	Input power on/off - suspend line of the system. Connect a 51 K pull-up to VCC_ MCA.
	3. Isolate VCC_MCA power domains	As much as possible, try not to mix the VCC_MCA power domain with the rest of the power domains of the system.
	4. MCA recovery	Digi recommends you enable access to the SWD port of the MCA in the carrier board. This will allow you to recover the MCA in case its firmware gets corrupted and the micro-controller can no longer boot.

Console debug port

☑	Item	Description
	1. UART2	The default U-Boot loaded in the modules from manufacturing configures the UART2 as the console debug port. This console port can be changed to any other UART in the system, but Digi recommends you use this UART2 as the console port so no additional effort (such as compiling a new U-Boot, loading it through USB, etc.) are required.

I2C

☑	Item	Description
	1. I2C pull-ups	Add external pull-ups to the clock and data lines of the I2C buses. You will typically use 4.7K resistors.

Wireless and Bluetooth

☑	Item	Description
	1. Wireless SDIO	Wireless SDIO is not used by the default wireless MAC populated on the ConnectCore 8X SOM. Leave these pads unconnected: D5, D6, D7, D8, D9, D10, D11, D12, D13, D14 and G18.

☑	Item	Description
	2. Bluetooth UART	The UART1 port of the CPU is used for Bluetooth connectivity internally in the SOM. The following pads must be left unconnected to preserve this Bluetooth functionality: ■ E13 (BT_UART1_TX) ■ E12 (BT_UART1_RX) ■ F12 (BT_UART1_CTS#) ■ F11 (BT_UART1_RTS#) This applies only to wireless variants of the SOM. In non-wireless variants, the UART1 bus is available.
	3. Not supported functionality	Functionality associated with the following pads is not currently supported: ■ B16: WLAN_RF_KILL# ■ B17: BT_RF_KILL# ■ F24: WLAN_LED ■ F26: BT_LED

CPU control lines

☑	Item	Description
	1. POR_B	POR_B is the reset line of the CPU. It is managed internally. It can be used as an output for managing (resetting) external circuitry of the carrier board. Do not drive it as an input unless otherwise noted (e.g, JTAG interface). Even though this signal is not used externally, it may be useful to have it accessible for debugging (test point).
	2. IMX8_ ON_OFF	By default, leave this pad unconnected.
	3. PWR_ ON	Similar to the POR_B signal, this line is driven internally in the SOM. It is the PMIC ON/OFF signal. It can be used externally for managing external circuitry but must never be driven as an input. Although this signal is not used externally, it may be helpful to leave it accessible for debugging (test points).
	4. SCU_ PMIC_ STANDBY	SCU_PMIC_STANDBY is the standby signal of the PMIC, and it is also controlled internally in the SOM. It can be used externally for managing external circuitry, but must never be driven as an input.

PCIe

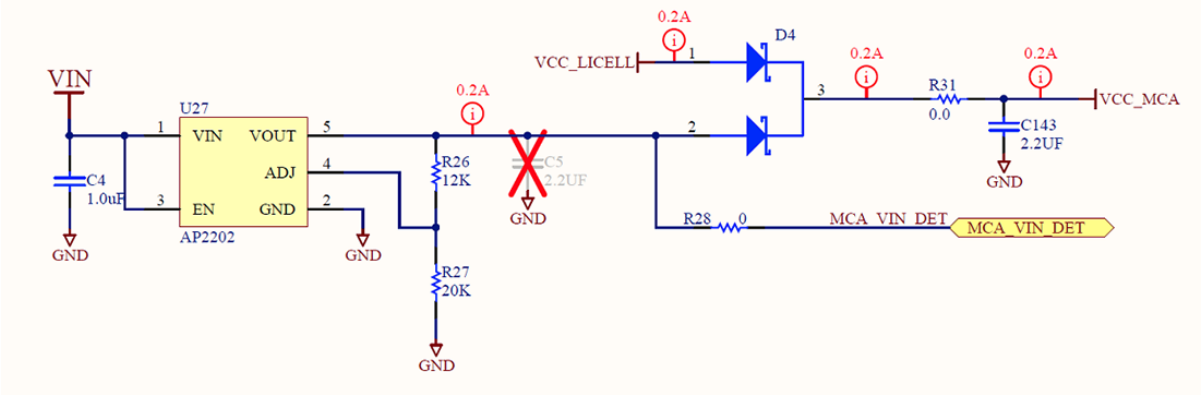
☑	Item	Description
	1. PCIe interface	PICe interface is used in the Wireless variants of the SOM to connect the Wireless MAC to the i.MX8X CPU. In non-wireless variants, this bus is available externally for general purpose: ■ Reference clock must be driven externally through the following pads: • G4: PCIE0_LGA_IN_REFCLK_P • G3: PCIE0_LGA_IN_REFCLK_N ■ Transmission data pair of the CPU (module output) is connected to the following pads: • G10: PCIE0_LGA_OUT_TX0_P • G9: PCIE0_LGA_OUT_TX0_N ■ Receiver data pair of the CPU (module input) is connected to the following pads: • G7: PCIE0_LGA_OUT_RX0_P • G6: PCIE0_LGA_OUT_RX0_N The remaining PCIe-related pads are unconnected in all variants: F4, F5, F6, F7, F8, F9, G20, G21, G23, G24. Leave this pins unconnected. Decoupling capacitors in the transmission data lines must be set externally.

ADCs

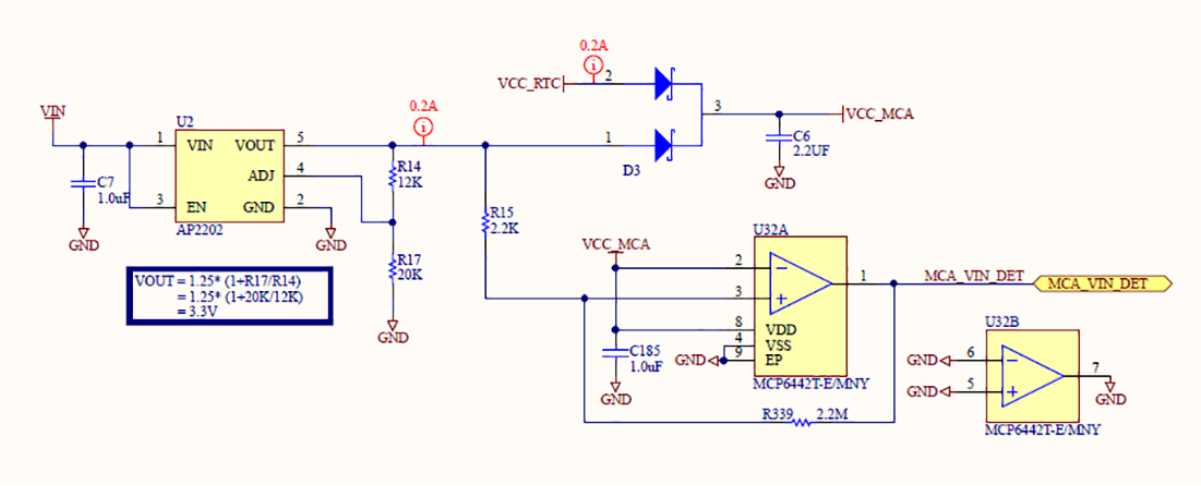
☑	Item	Description
	1. ADC_VREFH	Digi recommends you use VDD_ADC_1V8 as the CPU ADCs voltage reference; this means connecting VDD_ADC_1V8 (pad AG24) to ADC_VREFH (pad J29).

Schematics

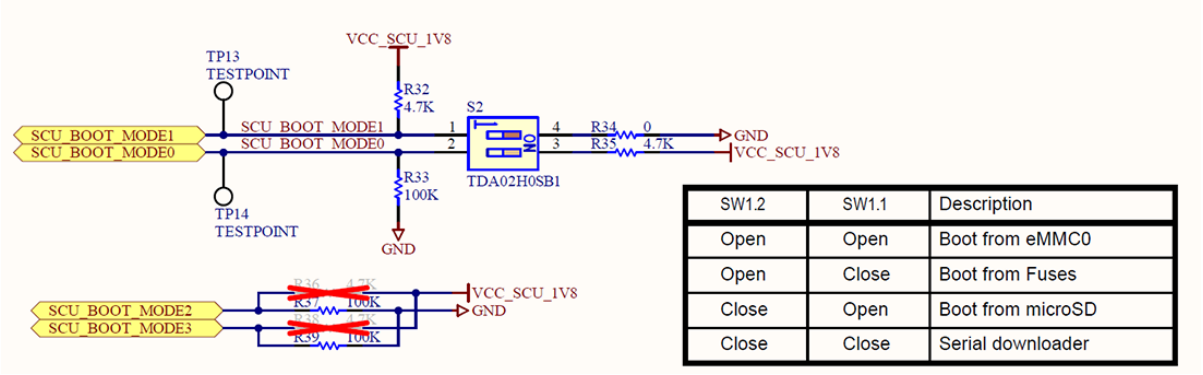
Coin-cell/supercap connected to VCC_MCA through Schottky diode



Comparator used for connecting MCA_VIN_DET line



Boot mode switches for selecting the boot source of the module



SW1.2	SW1.1	Description
Open	Open	Boot from eMMC0
Open	Close	Boot from Fuses
Close	Open	Boot from microSD
Close	Close	Serial downloader

Bring-up guidelines

This section offers guidelines for performing bring-up of a ConnectCore 8X-based product.

Power-up

The very first power-up of a product is one of the most critical step of the bring-up. Use a power supply with current limiter so the system is protected in case an unexpected short (or any other high-current incident) occurs. The SOM will not have a static power consumption higher than 200-250 mA from factory mode (except booting peaks). So, together with the expected power consumption of the carrier board, you can estimate an upper limit for the current consumption in the bring-up.

Power rails

Once you have verified that the power consumption of the system is acceptable and no shorts are present, the next step is to verify that all power rails also have their expected voltage value. The following table tracks the voltage expected in the main power domains of the system:

Power rail	Expected voltage
VSYS/VSYS2	5 V
VCC_MCA	3 V - 3.3 V (Output of the 3.3 V dedicated regulator minus Schottky diode forward voltage).
3V3	3.3 V
1V8	1.8 V
VCC_SCU_1V8	1.8 V
VDD_PCIE_DIG	3.3 V
VDD_EMMC0	3.3 V
NVCC_MIPI_CSI_DSI	1.8 V

If all these power rails are in compliance with their expected voltage value, it means that the system is completely powered. The PMIC has already initialized and the SOM should boot.

Verify system boot

If everything has gone right and the system has booted, you should be able to communicate with the SOM through the console port of the system. If this is not the case, check the following:

- Make sure the UART debug port lines are not crossed. Crossing the TX and RX lines of the console UART is a very common mistake.
- Verify the value of the BOOT_MODE lines.
- Verify that MCA_VIN_DET is at high level (3.3 V).
- Verify that POR_B signal is at high level.

Note For more information, see the ConnectCore 8X System-on-Module Hardware Reference Manual.